By now you probably have heard of dual- and multi-core processors. Both AMD and Intel released dual-core chips in 2005, and both have plans to release dozens more dual-core chip variations this year. In 2007 the chipmakers expect to introduce several multi-core chips, beginning with quad-core offerings.

We discussed Intel’s multi-core processors in the January 2006 issue of CPU (page 50). This month, we’ll focus on what AMD has planned for 2006 and beyond.

**Dual-Core Chips**

In April 2005, AMD released its first dual-core chip aimed at the server and workstation market, the Opteron processor. There are several Opteron dual-core 90nm processors ranging in clock speeds from 1.6GHz to 2.4GHz.

**Direct Connect Architecture vs. Legacy Systems**

Direct Connect Architecture lives up to its name by providing a direct connection between the processor, the memory controller, and the I/O area to improve overall system performance. AMD has used Direct Connect Architecture for the past few years in its single-core chips. But now AMD has extended the use of Direct Connect Architecture to connect the cores on a dual- or multi-core chip die and to connect each core to its memory controller.

When using a dual-processor x86 legacy architecture, however, two processors then have to share the same memory control hub, which creates bottlenecks in data transfers at the FSB. The two processors aren’t connected, either, which can lead to latency problems. With multi-core architecture, each core on the chip has its own memory controller, which significantly improves memory performance. Using Direct Connect Architecture to make a connection with the memory controller eliminates most bottlenecks and makes multitasking easier. Also, connecting the processor cores together lets data flow freely and reduces latency problems.

**Athlon 64 X2 Dual-Core Chips**

As with other families of AMD processors, a larger model number for an Athlon 64 X2 dual-core chip equals better software performance on that processor vs. those with smaller model numbers. Each Athlon 64 X2 90nm chip listed here runs at 1.35 to 1.40V and uses a Socket 939 socket.

<table>
<thead>
<tr>
<th>Processor</th>
<th>Clock Speed (GHz)</th>
<th>L2 Caches</th>
<th>Max Temp (°C)</th>
<th>Price*</th>
</tr>
</thead>
<tbody>
<tr>
<td>3800+</td>
<td>2</td>
<td>512KB (x2)</td>
<td>71</td>
<td>$328</td>
</tr>
<tr>
<td>4200+</td>
<td>2.2</td>
<td>512KB (x2)</td>
<td>65</td>
<td>$408</td>
</tr>
<tr>
<td>4400+</td>
<td>2.2</td>
<td>1MB (x2)</td>
<td>65 to 71</td>
<td>$507</td>
</tr>
<tr>
<td>4600+</td>
<td>2.4</td>
<td>512KB (x2)</td>
<td>65</td>
<td>$643</td>
</tr>
<tr>
<td>4800+</td>
<td>2.4</td>
<td>1MB (x2)</td>
<td>65</td>
<td>$803</td>
</tr>
</tbody>
</table>

*Price as of January 2006, for direct AMD customers in 1,000-unit quantities.
The first desktop dual-core processor from AMD appeared in May 2005 under the Athlon 64 X2 brand name. AMD has several variations of its Athlon 64 X2 processors. (See the “Athlon 64 X2 Dual-Core Chips” chart for some examples.) AMD’s first dual-core processors for notebooks and the mobile market should appear sometime in the first half of 2006. Multi-core processors from AMD should initially appear in 2007.

**Dual-Core Technologies**

As AMD releases its dual- and multi-core chips, the company will introduce and improve upon several technologies.

**Cool’n’Quiet.** When AMD’s system is running Cool’n’Quiet technology, it adjusts the speed of the system fan and the voltage and clock speed of the cores on the processor based on the system case temperature. (See the “Cool’n’Quiet Technology” sidebar for more information.)

**Direct Connect Architecture.** AMD plans to enhance this technology in dual- and multi-core chips to improve data transfer connections among the cores on the chip. (For more information see the “Direct Connect Architecture vs. Legacy Systems” sidebar.)

**HyperTransport 3.0.** AMD and the HyperTransport Consortium continue to develop HyperTransport 3.0, which may offer about three times the bandwidth of version 2.0. HyperTransport 2.0 can offer aggregate bandwidth up to 22.4GBps. As with previous versions of the technology, HyperTransport 3.0 will offer direct connections between the CPU and the I/O area. The new version will provide direct connections among the cores in the dual- and multi-core chips.

**AM2 socket technology.** During 2006 AMD will release new dual-core chips that use an AM2 socket technology, which uses a different pin configuration than AMD’s 939 socket. Customers who choose dual-core chips and motherboards that support the AM2 socket will then be able to upgrade to a quad-core chip, which also will use the AM2 socket when AMD introduces it (scheduled for 2007).

**Pacifica technology.** AMD’s Pacifica technology will improve performance, reliability, and security for virtualization hardware environments. It should appear in the first half of 2006 and use dedicated transistors to deliver the new features while running as part of dual- and multi-core chips. (See the “Using Pacifica Technology” sidebar for more information.)

**Presidio technology.** Presidio technology will give users advanced security features at the chip level. Although AMD has released very little information about how Presidio will work or when it may appear, think of Presidio as creating a protected area on the processor where it can store and process sensitive data.

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**Inside AMD’s Dual-Core Processor**

- **CPU 1 and CPU 2.** The dual AMD64 cores on this chip can run 32- and 64-bit computing simultaneously.
- **64KB I-Cache.** The L1 instruction internal caches offer low latency.
- **1MB L2 Cache.** The L2 second-level internal caches offer low latency.
- **Crossbar.** The crossbar makes the connection between each core and the I/O area and memory interfaces. The crossbar is a key component of the chip, letting the core access the data it needs to run software and perform calculations.
- **Integrated DDR Memory Controller.** This feature reduces the latency associated with accessing memory vs. using an FSB architecture to access memory. Each core has its own memory controller.
- **System Request Queue.** This area manages how each core accesses the crossbar switch.
- **Link 1/2/3.** These three links connect the I/O area to the processor using HyperTransport technology. HyperTransport also can provide a high-speed link among processors in a multi-processor configuration.
- **64KB D-Cache.** The L1 data internal caches are low latency.
- **72 bit.** This DDR400 memory interface provides data transfer rates up to 6.4GBps.

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Source: AMD
Multi-Core Benefits

Improved performance is pushing the migration to multi-core processors, but that’s not the only reason: Multi-core processors are also appearing out of necessity. The technological advances that have driven manufacturers to double the number of transistors on a chip every 18 to 24 months (fulfilling Moore’s Law) are beginning to reach their physical limits. Chipmakers have continually shrunk the manufacturing process for transistors over the years. They’re currently shifting the manufacturing process from 90 to 65nm, which lets them squeeze more transistors onto each chip. An IDC report, however, says that once the chip manufacturing process reaches about 16nm in size, the processors won’t be able to control the flow of electrons as the flow moves through the transistors. This means that transistors eventually will reach a size where chipmakers can no longer make them smaller. Ever smaller and denser transistors on a chip generate more heat, causing processing errors. But multi-core processors can improve computing power and limit some of the problems that shrinking transistors are causing.

The one drawback to multi-core technology is the increase in cost for systems and chips. However for many users the benefits will outweigh the cost factor.

A processor with two or more cores works faster and more efficiently than a single-core processor for several reasons:

- **Increased performance** in multitasking and running multiple applications at once.
- Users can add more computing power without the cost of adding another computer. This feature especially benefits commercial users, letting them add more processing power without adding more servers. By adding fewer servers, companies will need less real estate to hold the servers. Also, the costs of electrical power to run those servers and the cost of cooling the servers will decrease.
- For those who compile software code, dual- and multi-core processors seriously improve compiling efficiency. AMD says its current dual-core processors reduce the time needed to compile code by as much as 50% compared to a single-core processor.
- Game developers can add more features and cutting-edge graphics to their games because dual- and multi-core chips will more easily and efficiently handle multitask software designs.
- Multi-core processors don’t consume more power or generate more heat vs. a single-core processor, which will give users more processing power without the drawbacks typically associated with such increases.

### AMD’s Multi-Core Processor Future

When AMD designed the AMD64 processor during the late 1990s, the company had dual- and multi-core technologies in mind. Such planning has made AMD’s evolution into multi-core products an easier process. For example, AMD designed some of its current dual-core processors to fit in the same sockets as its single-core offerings, such as the 940-pin Opteron processor and the 950-pin Athlon 64 processor. Also, all of the software that runs under Win and AMD64 processors will work with AMD’s multi-core processors; no coding changes needed.

During the past couple of years, AMD has moved away from releasing timelines listing detailed plans for its future processors complete with code names. Instead, AMD’s beginning to give more general names to overall chip projects, rather than splitting out code names for individual chip plans.

**K8 Dual Core.** This is the server and workstation Opteron dual-core chip that debuted in April 2005. **K8L.** This quad- or eight-core chip will potentially follow K8 in 2007 or 2008, although little is known about this project. **K9.** Due to launch in late 2007, K9 should be a quad-core chip appearing under the Opteron brand name in servers. It will feature a new core design, DDR3 memory, and contain L3 cache, which will let server designers build systems using up to 32 processors. (Current cache settings allow for only eight processors per system.) AMD road maps indicate quad-core chips for desktops will initially appear in 2008. **Santa Rosa.** This dual-core chip should be part of the Opteron 100 series, use an AMD socket, and appear in the second half of 2006.

**Santa Rosa: Expected to appear in the first half of 2006, this dual-core chip should be part of the Opteron 100/200 series.**

**Trinidad.** Due sometime in 2006 and intended for the mobile market, this 90nm AMD64 dual-core chip will use an AMD socket.

**Windermere.** This 65nm dual-core chip should appear early in 2006, use an AMD socket, and support DDR2 memory.
Virtualization uses software to share and manage workloads at the processor level, making it appear as though the server contains a multi-processor system. A single server can run multiple OSes and applications using virtualization. Implementing the idea of virtualization also means companies don’t need to have as much hardware performance capability held in reserve among their servers to meet peak situations.

By building virtualization technology inside the processor, as AMD will do with Pacifica technology, multi-core processors could then provide better overall performance vs. a single-core processor trying to run virtualization. Pacifica, which AMD will introduce later this year, would simplify the implementation of virtualization and let it more easily take advantage of the multiple cores on a processor.

In a system without Pacifica technology, the x86 processor hardware contains no virtualization capabilities. When creating a virtual machine in this type of system, the virtualization software must manage the resources between the host OS and the guest OS. Because this extra layer causes additional overhead and complexity, application performance suffers.

With Pacifica running on an AMD dual- or multi-core processor, there would be fewer layers and less complexity, improving application performance. Pacifica would use Hypervisor as its virtualization software, which would manage the virtual machines. Hypervisor also would track the availability of physical hardware, letting applications take advantage of the hardware as it becomes available.

AMD has carried its Cool’n’Quiet technology into its dual-core offerings. It cuts down on the heat and noise that a processor generates and helps the processor use less power by cutting back on the its clock speed and voltage when the computer user’s demands are less. AMD says users rarely will notice any system performance degradation while using Cool’n’Quiet because it can adjust the clock speed and voltage up to 30 times per second.

To run Cool’n’Quiet, a PC needs a heatsink with a variable speed fan, which adjusts the fan’s rotation speed based on the computer case’s air temperature. The system also needs a Cool’n’Quiet driver.

When running Cool’n’Quiet, the CPU operates in one of three basic states: maximum, intermediate, or minimum. The intermediate state can have more than one setting, and the more settings available, the more flexibility the processor has to save power and reduce heat. For example, AMD’s Athlon 64 3500+ processor can operate in one of four states, measured by the clock speed and voltage it uses:

- **Maximum**: 2.2GHz; 1.5V
- **Intermediate A**: 2GHz; 1.4V
- **Intermediate B**: 1.8GHz; 1.3V
- **Minimum**: 1GHz; 1.1V

The minimum state works well for computing tasks involving a lot of idle processor time, such as word processing and emailing. Intermediate states work well for tasks requiring a lot of continuous processor access, such as system scans with no other tasks occurring or processes running.

As the Cool’n’Quiet driver works with the motherboard to measure system temperature and current processor workload (based in part on the type of software a user is running), it places the processor in the most appropriate state. At the same time, the variable speed fan speeds up or slows down to match the change in the processor’s state. As the processor decreases its clock speed and uses less power, the processor and power supply generate less heat. As the temperature in the case falls, the system can decrease the fan’s rotation speeds, leading to less noise from the fan and from air turbulence.

In contrast, when a user cranks up system performance to the maximum state, Cool’n’Quiet increases the fan’s rotation speed to remove the additional heat it now generates, increasing system noise.